ABSTRACT

A memory cell transistor includes a high dielectric constant tunnel insulator, a metal floating gate, and a high dielectric constant inter-gate insulator comprising a metal oxide formed over a substrate. The tunnel insulator and inter-gate insulator have dielectric constants that are greater than silicon dioxide. Each memory cell has a plurality of doped source/drain regions in a substrate. A pair of transistors in a row are separated by an oxide isolation region comprising a low dielectric constant oxide material. A control gate is formed over the inter-gate insulator.